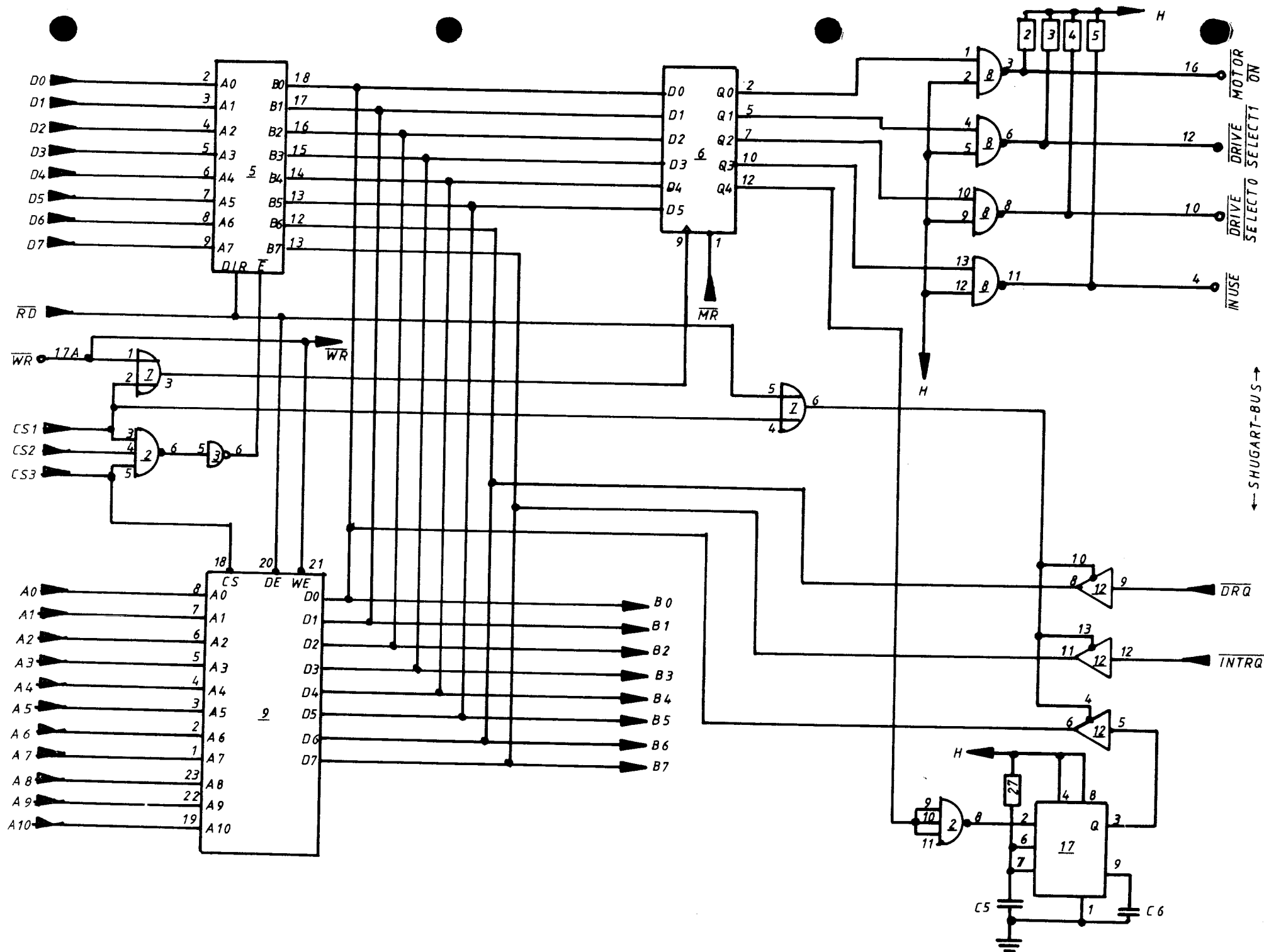


CS 0 = 2000h-27FFh  $\triangleq$  EPROM

CS 1 = 2800h-2FFFh  $\triangleq$  D-Register

CS 2 = 3000h-37FFh  $\triangleq$  FDC

CS 3 = 3800h-3FFFh  $\triangleq$  RAM



READ DATA  
30

WPRT  
28

TR00  
26

IP  
8

WG  
24

WD  
22

STEP  
20

DIRC  
18

← SHUGART-BUS

H.

B0

B1

B2

B3

B4

B5

B6

B7

A0

A1

CS2

RD

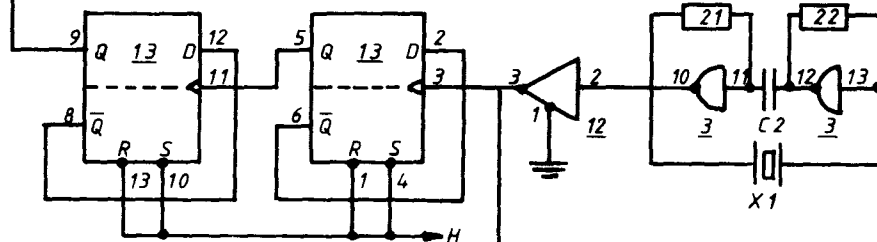
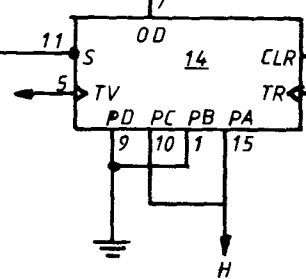
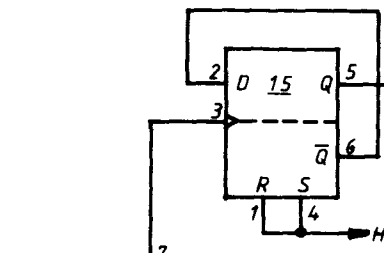
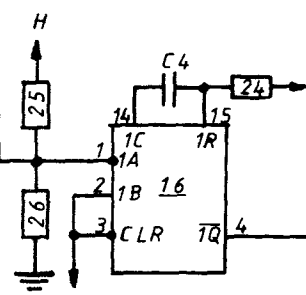
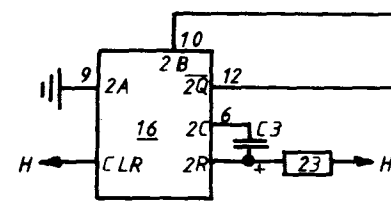
WR

DRQ

INTRQ

RESET

IC 10



## Bedienungsanleitung zum FDC:

Das Betriebssystem des FDC ist auf der Platine in einem EPROM untergebracht und umfaßt folgende Funktionen mit den danebenstehenden Aufrufen

Directory	RAND USR 8195
Format	RAND USR 8192
Erase	RAND USR 8204
Save	RAND USR 8198
Load	RAND USR 8201

Formatiert werden 80 Spuren mit je 16 Sektoren. Die Speicherkapazität beträgt nach dem Formatieren einseitig 158 KB. Die vorliegende Version unterstützt nur das Benützen von einer Diskettenseite. Durch Hardwareeingriffe können auch beide Seiten benützt werden.

Es können alle 3 1/2"-Laufwerke mit Shugart-Bus verwendet werden.

Es können maximal 64 Programme gespeichert werden. Das Speichern von Dateien ist nur mit dem Hilfsprogramm FILE möglich.

Der Aufruf der Funktionen ist durch die direkte Befehlseingabe oder aus einer BASIC-Zeile heraus möglich. Das automatische Laden oder Saven aus einem BASIC-Programm heraus geschieht mit folgenden Zeilen:

Laden: LET N\$="NAME...." (8 Buchstaben, evtl. mit Space auf füllen!)

```
FOR I=1 TO 8
POKE (14722+I), CODE N$(I TO I)
NEXT I
RAND USR 9187
RAND USR 9041
```

Saven: LET N\$="NAME...."

```
FOR I=1 TO 8
POKE (14722+I), CODE N$(I TO I)
NEXT I
RAND USR 8684
```

## Wichtiger Hinweis zum Aufbau der Platine:

Die Betriebssicherheit erhöht sich, wenn an alle IC an deren Spannungsversorgungs-Pins 10 bis 100 nF-Kondensatoren angebracht werden.

3

READ DATA

Read Data

WPRTP

READY  
nicht benutzt

WPRTP →

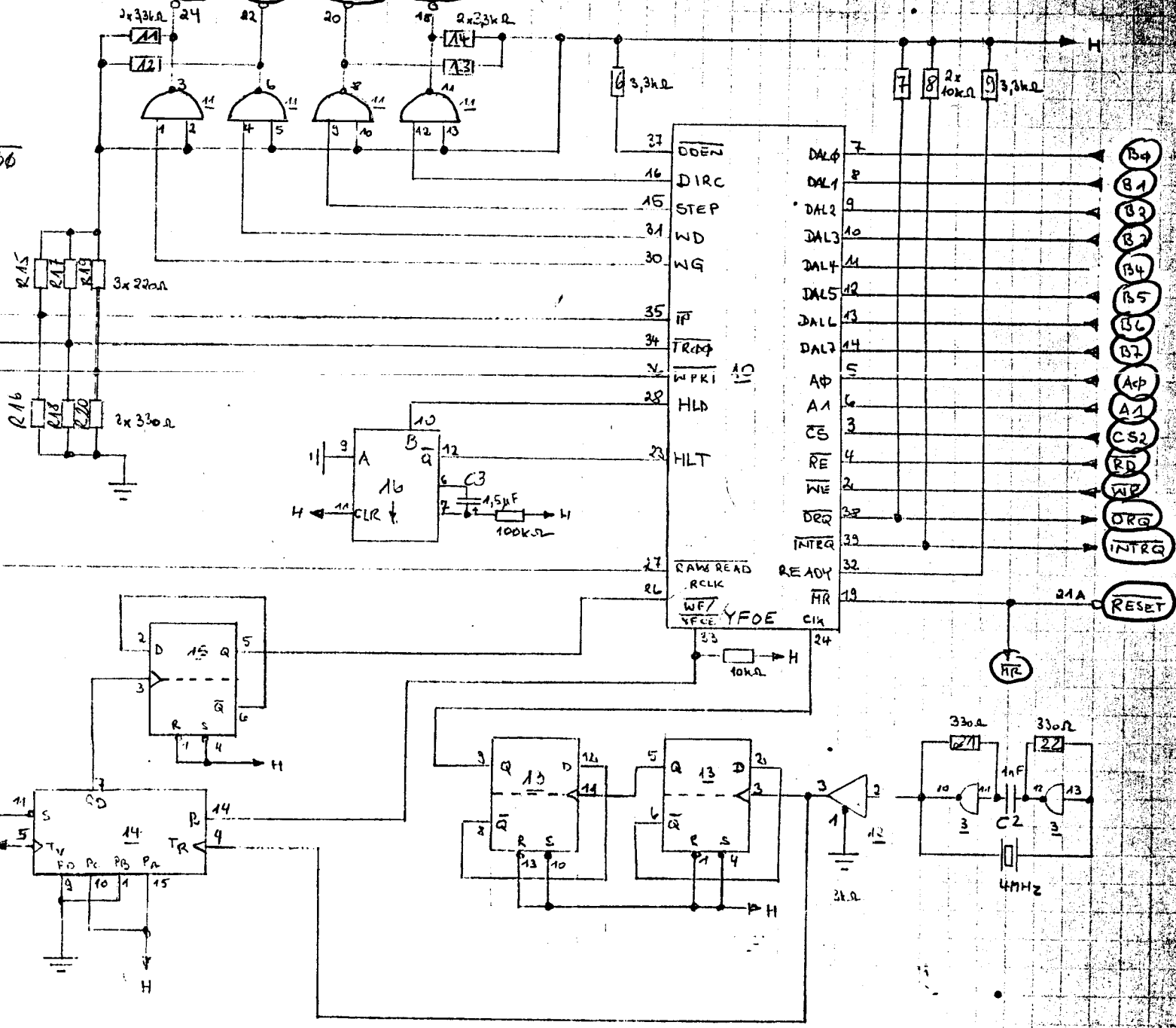
WG

WD

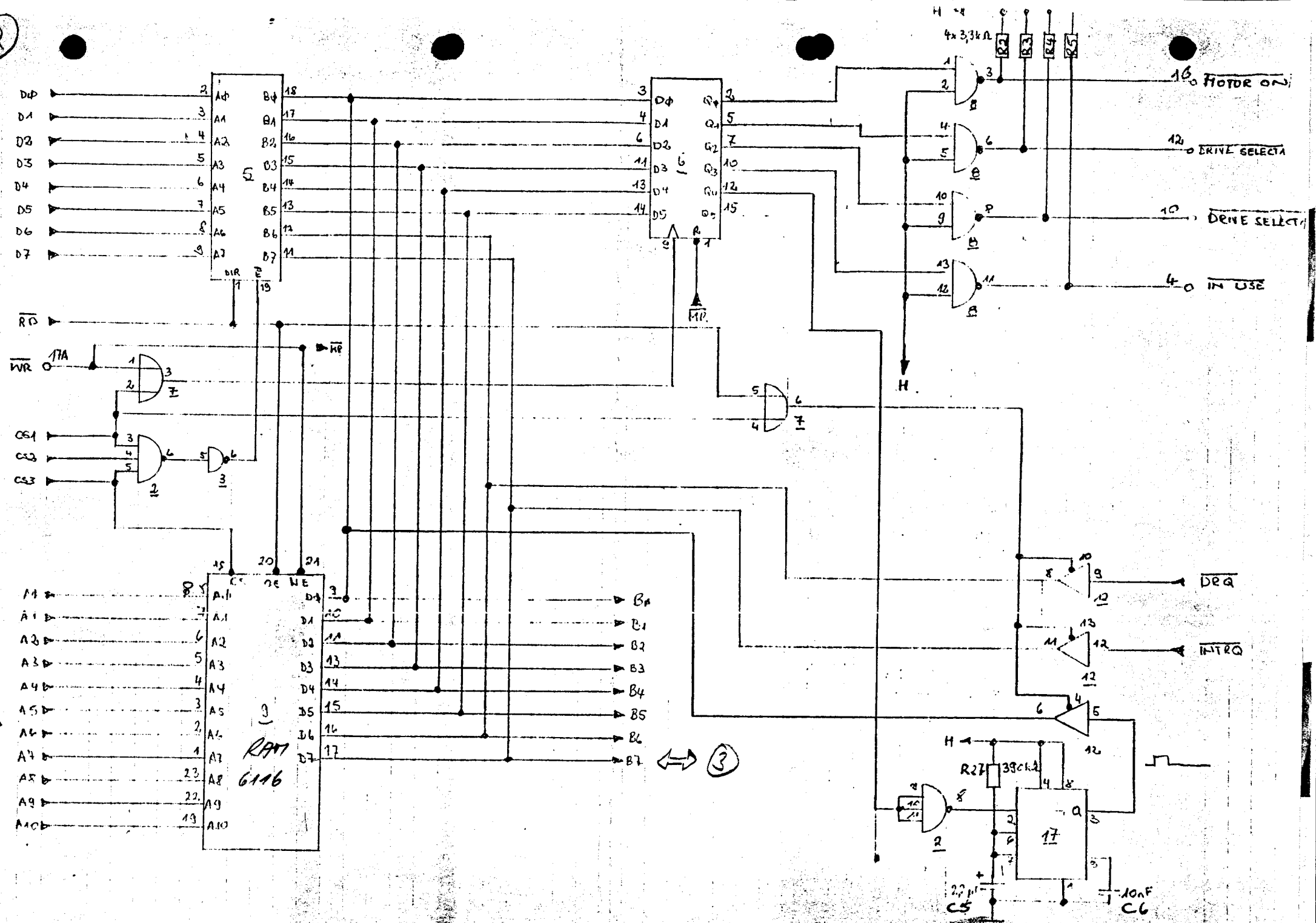
STEP

DIRC

← Sugarf Bus



Arbeitsblätter



⑦



2716

# FD 179X-02 Floppy Disk Formatter/Controller Family

## FD 179X-02 Floppy Disk Formatter/Controller Family

### FEATURES

- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS  
IBM 3740 Single Density (FM)  
IBM System 34 Double Density (MFM)
- READ MODE  
Single/Multiple Sector Read with Automatic Search or Entire Track Read  
Selectable 128 Byte or Variable length Sector
- WRITE MODE  
Single/Multiple Sector Write with Automatic Sector Search  
Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY  
Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status  
DMA or Programmed Data Transfers  
All Inputs and Outputs are TTL Compatible  
On-Chip Track and Sector Registers/Comprehensive Status Information

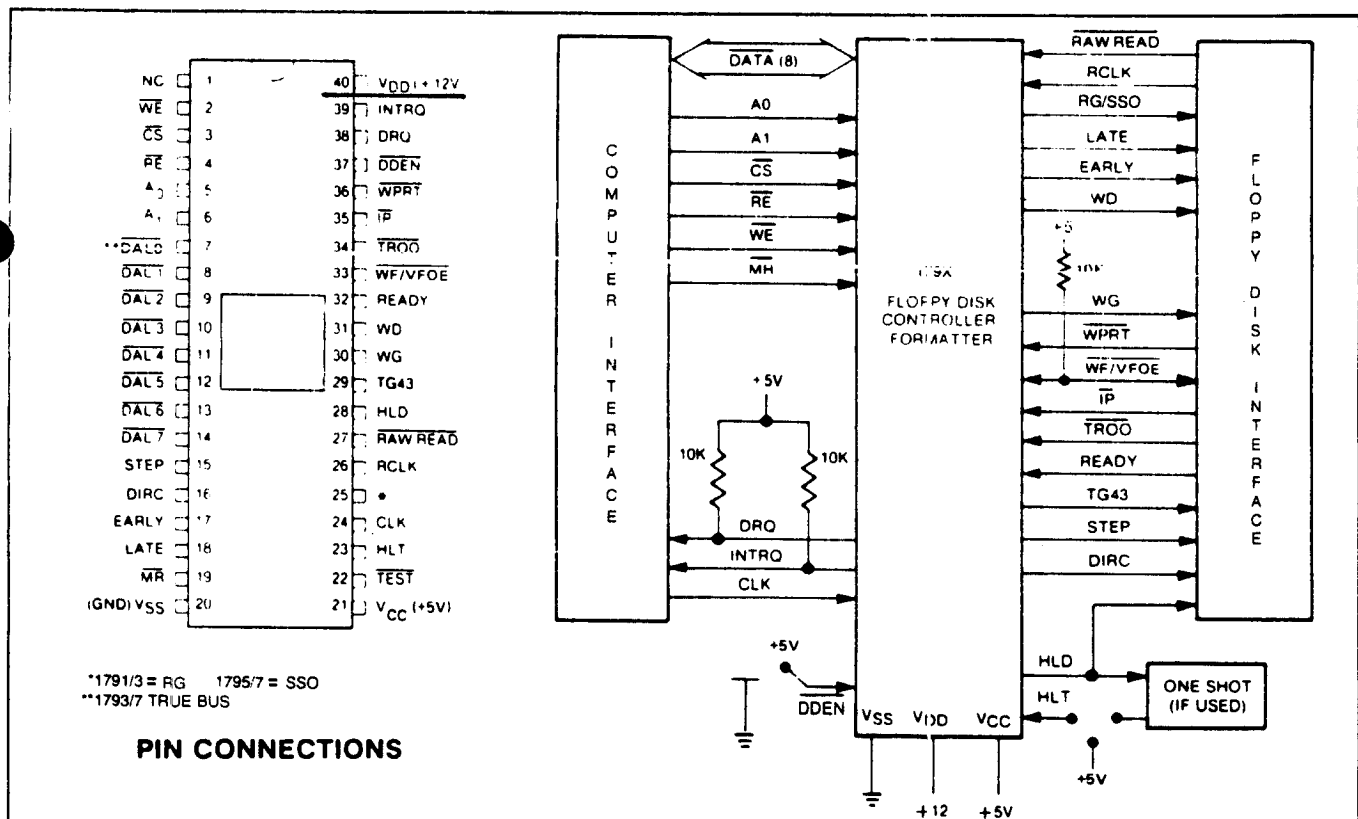
- PROGRAMMABLE CONTROLS  
Selectable Track to Track Stepping Time  
Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

### 179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

### APPLICATIONS

FLOPPY DISK DRIVE INTERFACE  
SINGLE OR MULTIPLE DRIVE CONTROLLER/  
FORMATTER  
NEW MINI-FLOPPY CONTROLLER



FD179X SYSTEM BLOCK DIAGRAM



## GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load

control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

## PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION																				
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.																				
19	MASTER RESET	$\overline{\text{MR}}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.																				
20	POWER SUPPLIES	V <sub>SS</sub>	Ground																				
21		V <sub>CC</sub>	+5V ±5%																				
40		V <sub>DD</sub>	+12V ±5%																				
COMPUTER INTERFACE:																							
2	WRITE ENABLE	$\overline{\text{WE}}$	A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.																				
3	CHIP SELECT	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.																				
4	READ ENABLE	$\overline{\text{RE}}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.																				
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control: <table><tr><td>A1</td><td>A0</td><td><math>\overline{\text{RE}}</math></td><td><math>\overline{\text{WE}}</math></td></tr><tr><td>0</td><td>0</td><td>Status Reg</td><td>Command Reg</td></tr><tr><td>0</td><td>1</td><td>Track Reg</td><td>Track Reg</td></tr><tr><td>1</td><td>0</td><td>Sector Reg</td><td>Sector Reg</td></tr><tr><td>1</td><td>1</td><td>Data Reg</td><td>Data Reg</td></tr></table>	A1	A0	$\overline{\text{RE}}$	$\overline{\text{WE}}$	0	0	Status Reg	Command Reg	0	1	Track Reg	Track Reg	1	0	Sector Reg	Sector Reg	1	1	Data Reg	Data Reg
A1	A0	$\overline{\text{RE}}$	$\overline{\text{WE}}$																				
0	0	Status Reg	Command Reg																				
0	1	Track Reg	Track Reg																				
1	0	Sector Reg	Sector Reg																				
1	1	Data Reg	Data Reg																				
7-14	DATA ACCESS LINES	$\overline{\text{DAL0-DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{\text{VE}}$ or transmitter enabled by $\overline{\text{RE}}$ .																				
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.																				

Ariadne Layout System 3.0

(c) kls & Franzis-Verlag 1986

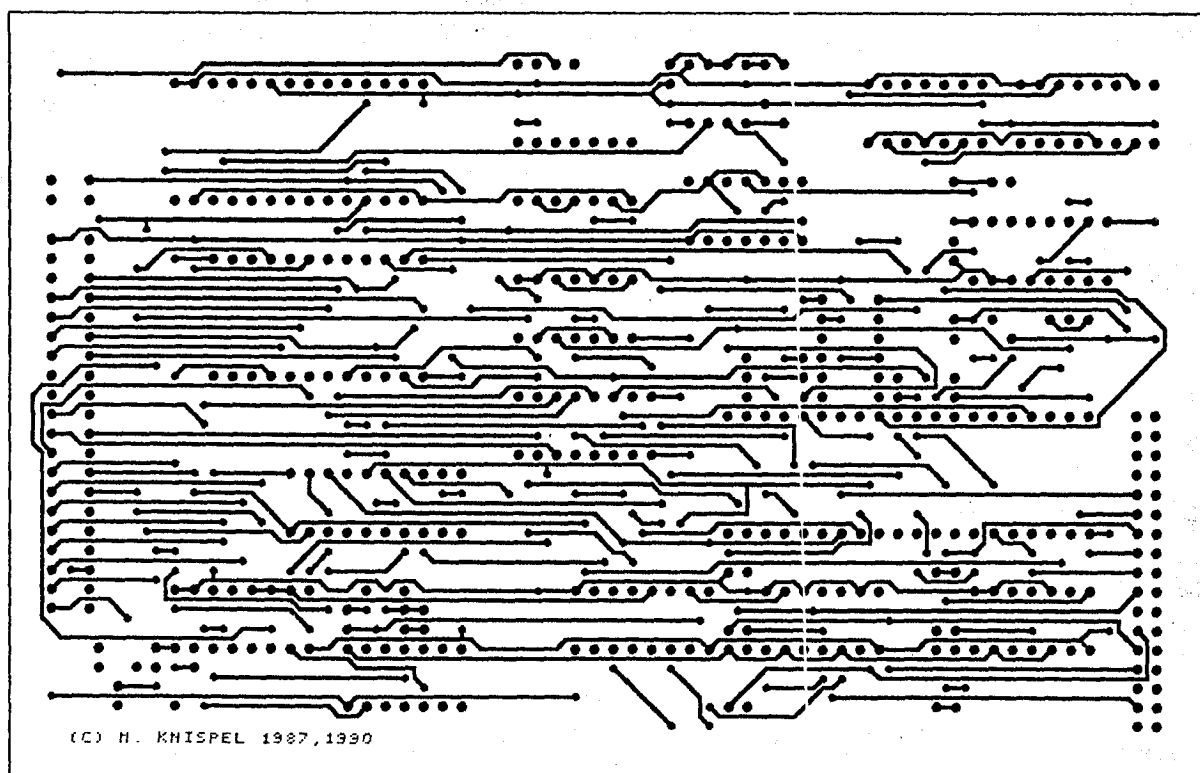
Platinenname : ZX81FDC

Bemerkung : Floppy-Controller für ZX81

Format : 100.0 \* 160.0 mm ( 76 \* 123 RE)

Masstab : 1.00 : 1 ( 9. Jul 1990 23:54:41)

BEST



Ariadne Layout System 3.0

(c) kls & Franzis-Verlag 1986

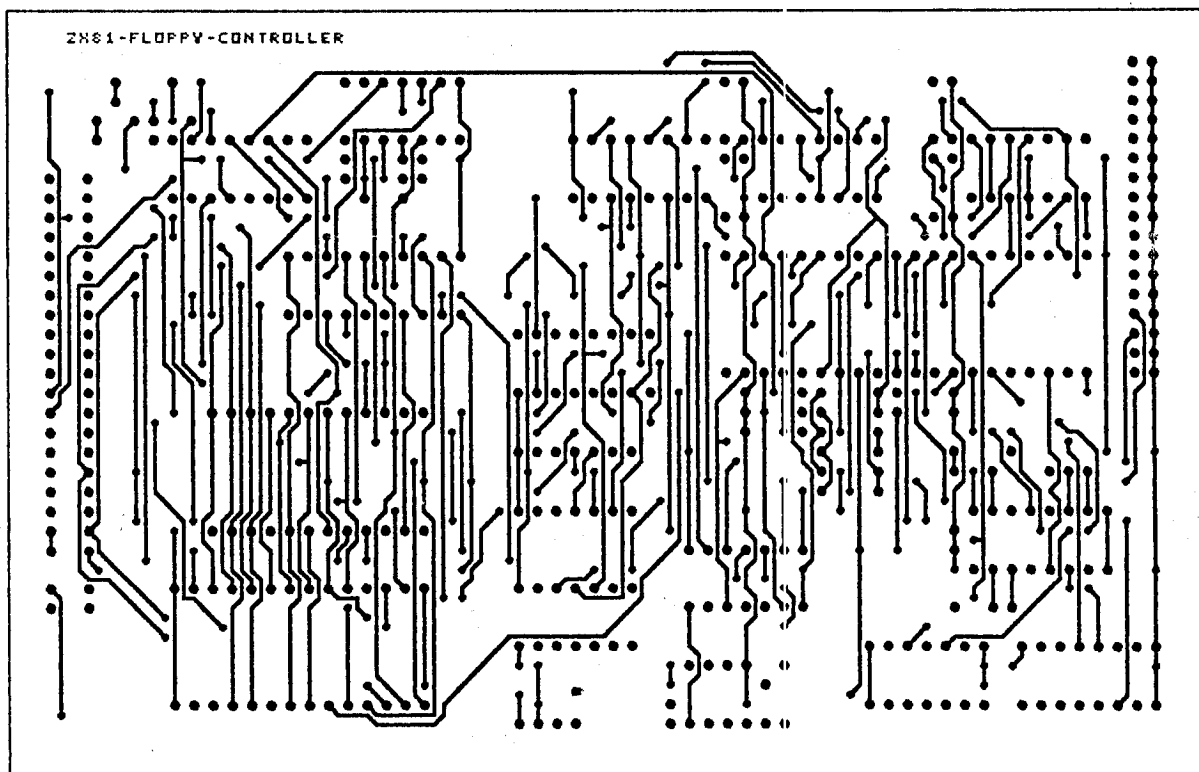
Platinenname : ZX81FDC

Bemerkung : Floppy-Controller für ZX81

Format : 100.0 \* 160.0 mm ( 76 \* 123 RE)

Masstab : 1.00 : 1 ( 9. Jul 1990 23:43:59)

LOET



Ariadne Layout System 3.0

(c) kls & Franzis-Verlag 1986

Platinenname : ZX81FDC

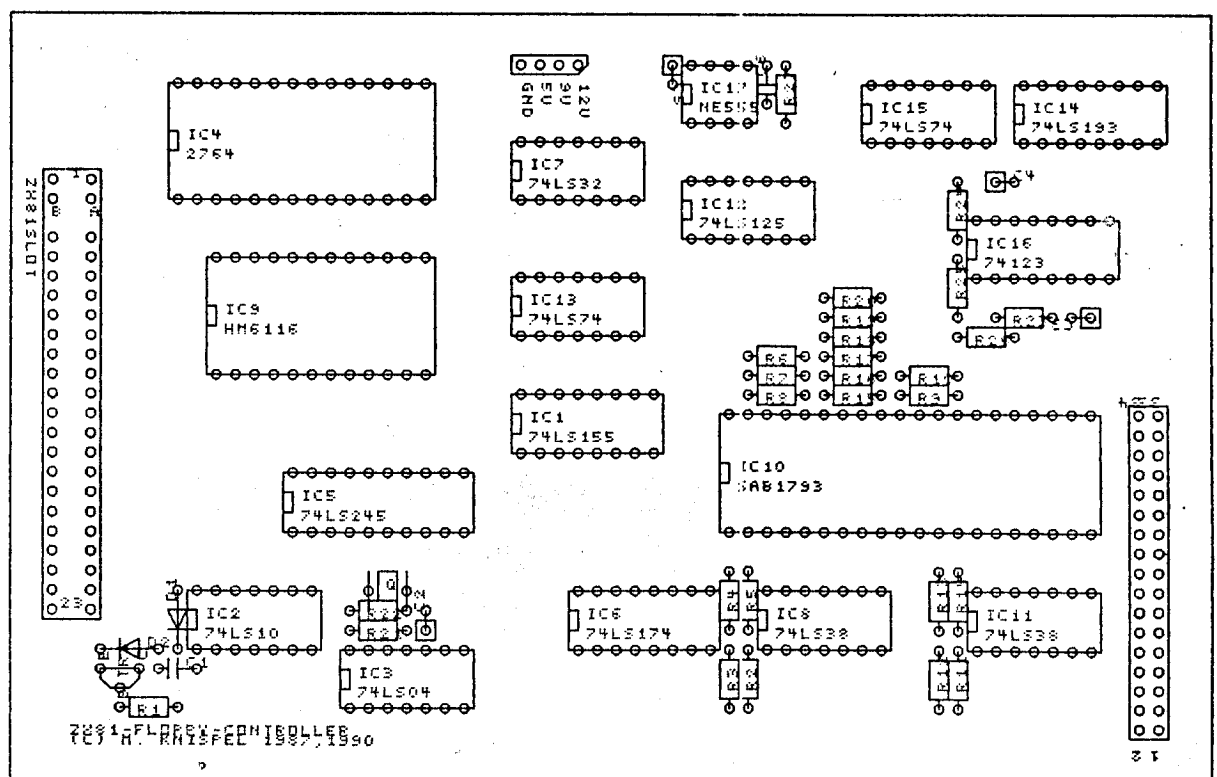
Bemerkung : Floppy-Controller für ZX81

Format : 100.0 \* 160.0 mm ( 76 \* 123 RE)

Masstab : 1.00 : 1 (10. Jul 1990 13:44:51)

BEPL

PINS



Ariadne Layout System 3.0

(c) kls & Franzis-Verlag 1986

Platinenname : ZX81FDC

Bemerkung : Floppy-Controller für ZX81

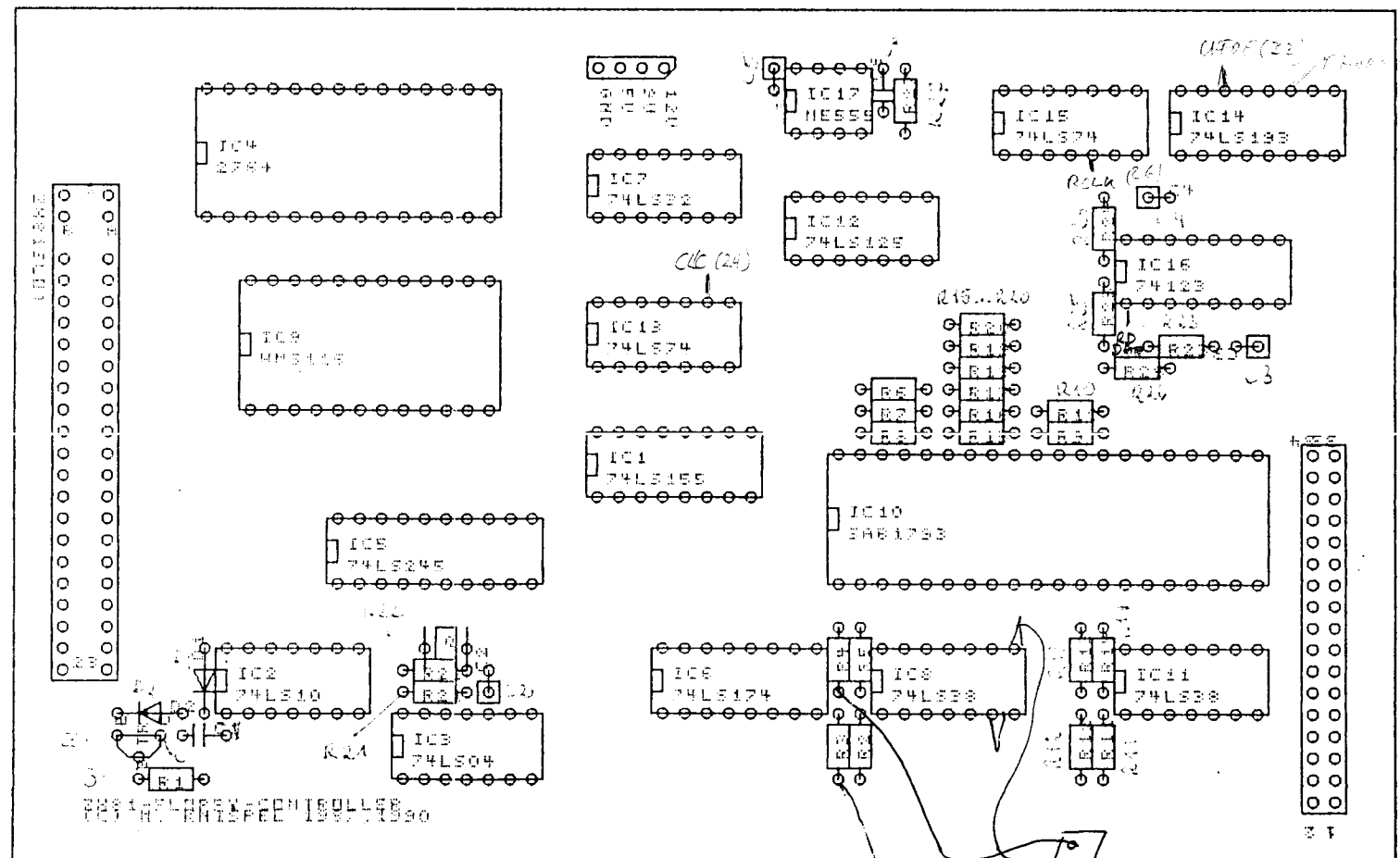
Format : 100.0 \* 160.0 mm ( 76 \* 123 RE)

Masstab : 1.00 : 1

(10. Jul 1990 13:44:51)

BEPL

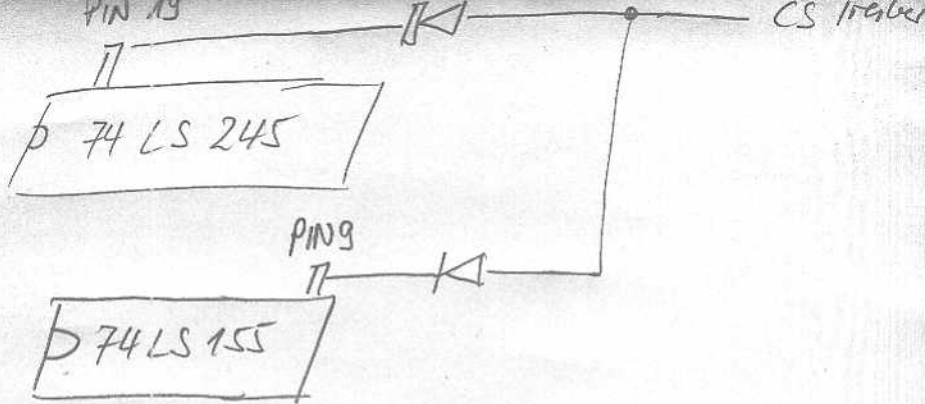
PINS



MENGE	BEZEICHNUNG		MENGE	BEZEICHNUNG	MENGE	BEZEICHNUNG
1	WIDERSTAND R1	10.2 K	1	C1 100 PF	1	IC1 74LS155
1	WIDERSTAND R2	4.4 K	1	C2 1 NF	1	IC2 74LS10
1	WIDERSTAND R3	4.4 K	1	C3 3.3 UF	1	IC3 74LS04
1	WIDERSTAND R4	4.4 K	1	C4 1 PF	1	IC4 2716
1	WIDERSTAND R5	4.4 K	1	C5 3.3 UF	1	IC5 74LS245
1	WIDERSTAND R6	4.4 K	1	C6 10 NF	1	IC6 74LS174
1	WIDERSTAND R7	10.2 K			1	IC7 74LS32
1	WIDERSTAND R8	10.2 K			1	IC8 74LS38
1	WIDERSTAND R9	4.4 K	1	D1 1N 4148	1	IC9 RAM-6116
1	WIDERSTAND R10	10.2 K	1	D2 1N 4148	1	IC10 SAB-1793
1	WIDERSTAND R11	4.4 K			1	IC11 74LS38
1	WIDERSTAND R12	4.4 K			1	IC12 74LS125
1	WIDERSTAND R13	4.4 K			1	IC13 74LS74
1	WIDERSTAND R14	4.4 K	1	T1 BC 307	1	IC14 74LS193
1	WIDERSTAND R15	220 OHM			1	IC15 74LS74
1	WIDERSTAND R16	350 OHM			1	IC16 74123
1	WIDERSTAND R17	220 OHM			1	IC17 NE555
1	WIDERSTAND R18	350 OHM	1	Q1 4 MHZ		
1	WIDERSTAND R19	220 OHM				
1	WIDERSTAND R20	350 OHM	1	IC-SOCKEL 8 POL		
1	WIDERSTAND R21	350 OHM	8	IC-SOCKEL 14 POL		
1	WIDERSTAND R22	350 OHM	4	IC-SOCKEL 16 POL		
1	WIDERSTAND R23	56 K	1	IC-SOCKEL 20 POL		
1	WIDERSTAND R24	30 K	2	IC-SOCKEL 24 POL		
1	WIDERSTAND R25	220 OHM	1	IC-SOCKEL 40 POL		
1	WIDERSTAND R26	350 OHM				
1	WIDERSTAND R27	390 K				

ZX-STECKERLEISTE  
FDC-STECKER  
STECKVERB. 4POL  
FDC-PLATINE 2-SEITIG





Freigabe FDC - Treiberplatine